

AFSC5G35D37 3400-3600 MHz REFERENCE CIRCUIT

ORDERABLE PART NUMBER: **AFSC5G35D37-EVB**



PUBLIC



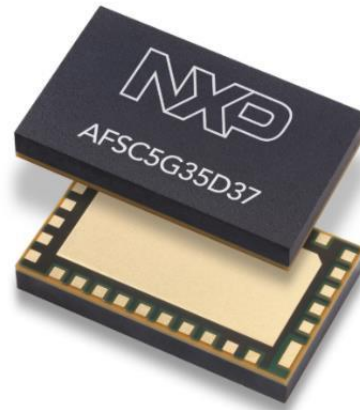
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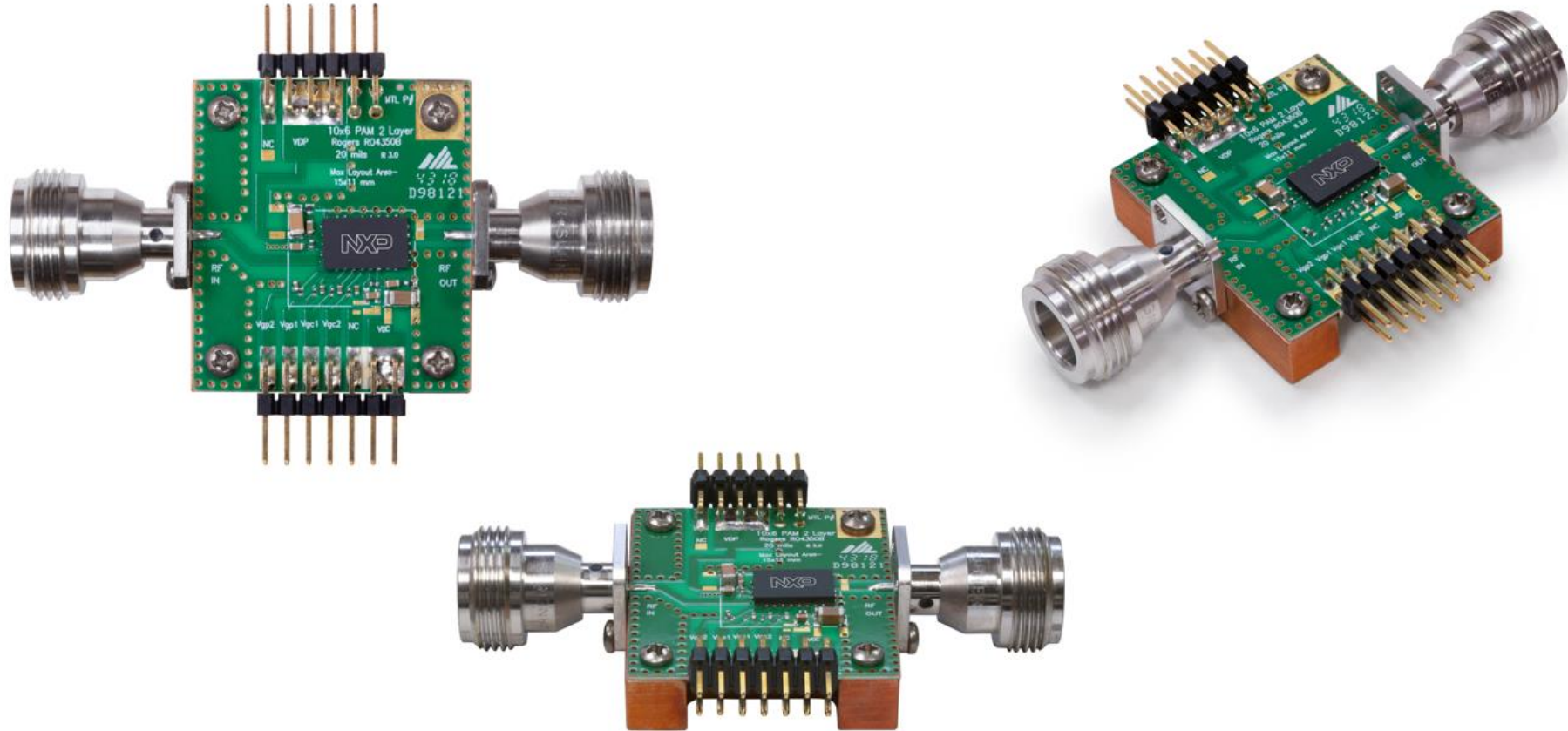
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Introduction

- The NXP AFSC5G35D37 is a 3400-3600 MHz, 5 W average RF power multi-chip module housed in a 10 mm x 6 mm LGA package. Its 50 ohm fully matched input and output ensures a small PA footprint.
 - Further details about the device, including its data sheet, are available [here](#).
- The following pages describe the 3400-3600 MHz reference circuit.
Its typical application is 5G 64T64R mMIMO active antenna systems for cellular base stations.
- The reference circuit can be ordered through NXP's distribution partners and etailers using part number AFSC5G35D37-EVB.



Circuit Overview – 3.30 cm × 3.71 cm (1.30" × 1.46")



Typical Performance 1/2

Typical LTE Performance: $P_{out} = 5 \text{ W Avg.}$, 1 x 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3400 MHz	29.2	-31.4	38.8
3500 MHz	29.3	-32.8	39.2
3600 MHz	29.4	-31.0	38.6

Operating conditions: $V_{DDc} = V_{DDp} = 30 \text{ Vdc}$, $I_{DQc1} = 17.5 \text{ mA}$, $I_{DQc2} = 60.5 \text{ mA}$, $V_{GGp1} = 1.7 \text{ Vdc}$, $V_{GGp2} = 1.4 \text{ Vdc}$
All data measured in fixture with device soldered in reference circuit.

Typical Performance 2/2

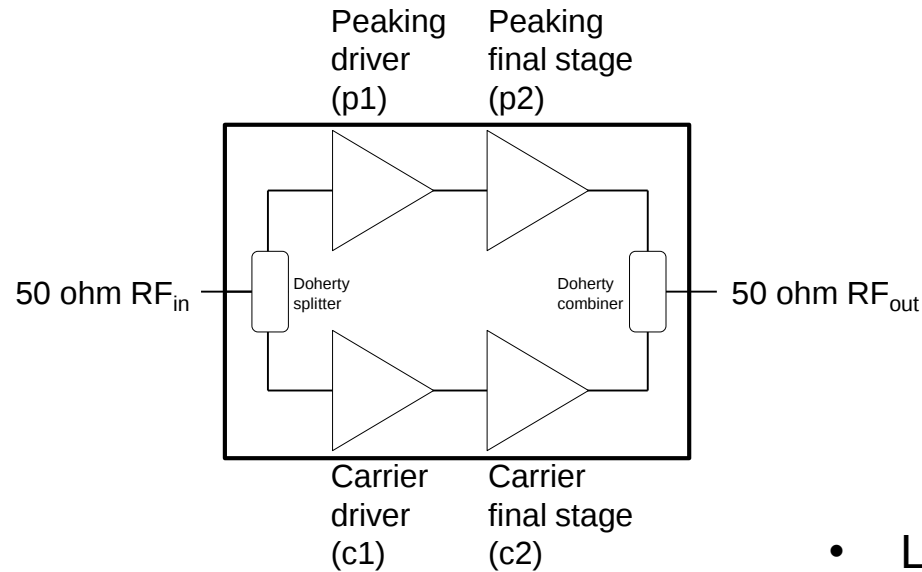
Operating conditions: $V_{DDc} = V_{DDp} = 30 \text{ Vdc}$, $I_{DQc1} = 17.5 \text{ mA}$, $I_{DQc2} = 60.5 \text{ mA}$, $V_{GGp1} = 1.7 \text{ Vdc}$, $V_{GGp2} = 1.4 \text{ Vdc}$, $P_{out} = 5 \text{ W Avg.}$, 3500 MHz

VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	300	—	MHz
Quiescent Current Accuracy over Temperature ⁽⁵⁾ with 2.2 k Ω Gate Feed Resistors (–40 to 85°C) Stage 1	ΔI_{QT}	—	1.0	—	%
with 2.2 k Ω Gate Feed Resistors (–40 to 85°C) Stage 2		—	2.0	—	
1-carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	29.3	—	dB
Power Added Efficiency	PAE	—	39.2	—	%
Adjacent Channel Power Ratio	ACPR	—	–32.8	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–44.6	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–53.0	—	dBc
Output Peak-to-Average Ratio @ 0.01% Probability	PAR	—	8	—	dB
Gain Flatness ⁽⁶⁾	G _F	—	0.2	—	dB
Fast CW, 27 ms Sweep					
P _{out} @ 3 dB Compression Point	P3dB	—	45.6	—	dBm
AM/PM @ P3dB	Φ	—	–25	—	°
Pulsed CW, 10 μsec(on), 10% Duty Cycle @ P1dB					
Gain Variation over Temperature (–40°C to +105°C)	ΔG	—	0.023	—	dB/°C
Output Power Variation over Temperature (–40°C to +105°C)	$\Delta P1dB$	—	0.01	—	dB/°C

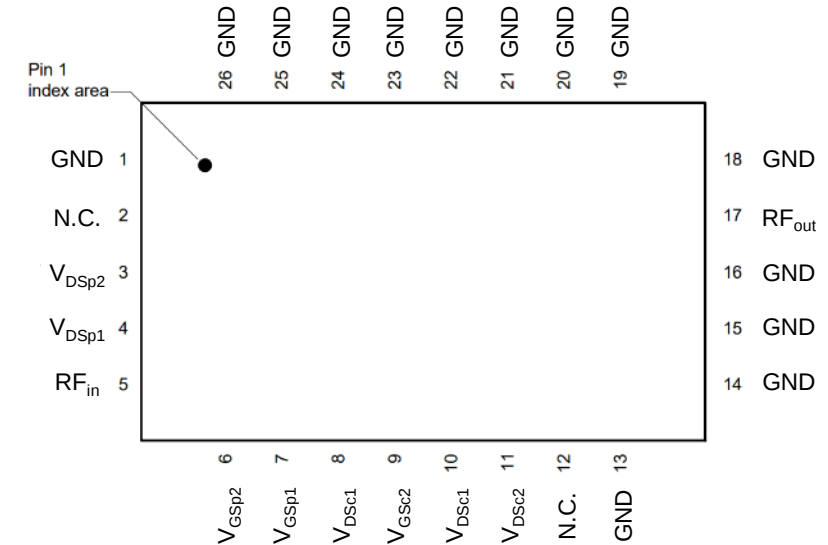
All data measured in fixture with device soldered in reference circuit.

Component Connection Details

- Functional Block Diagram:



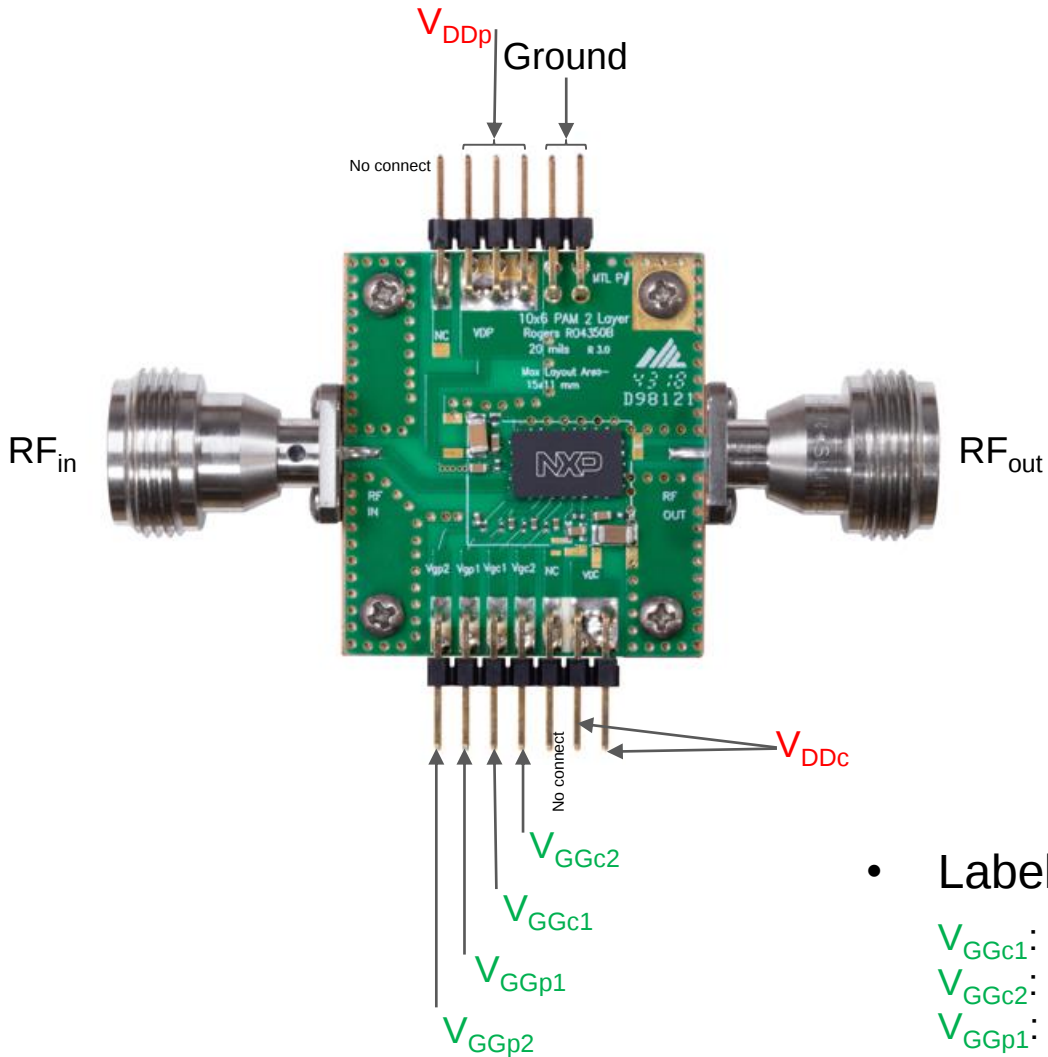
- Pin Connections (top view):



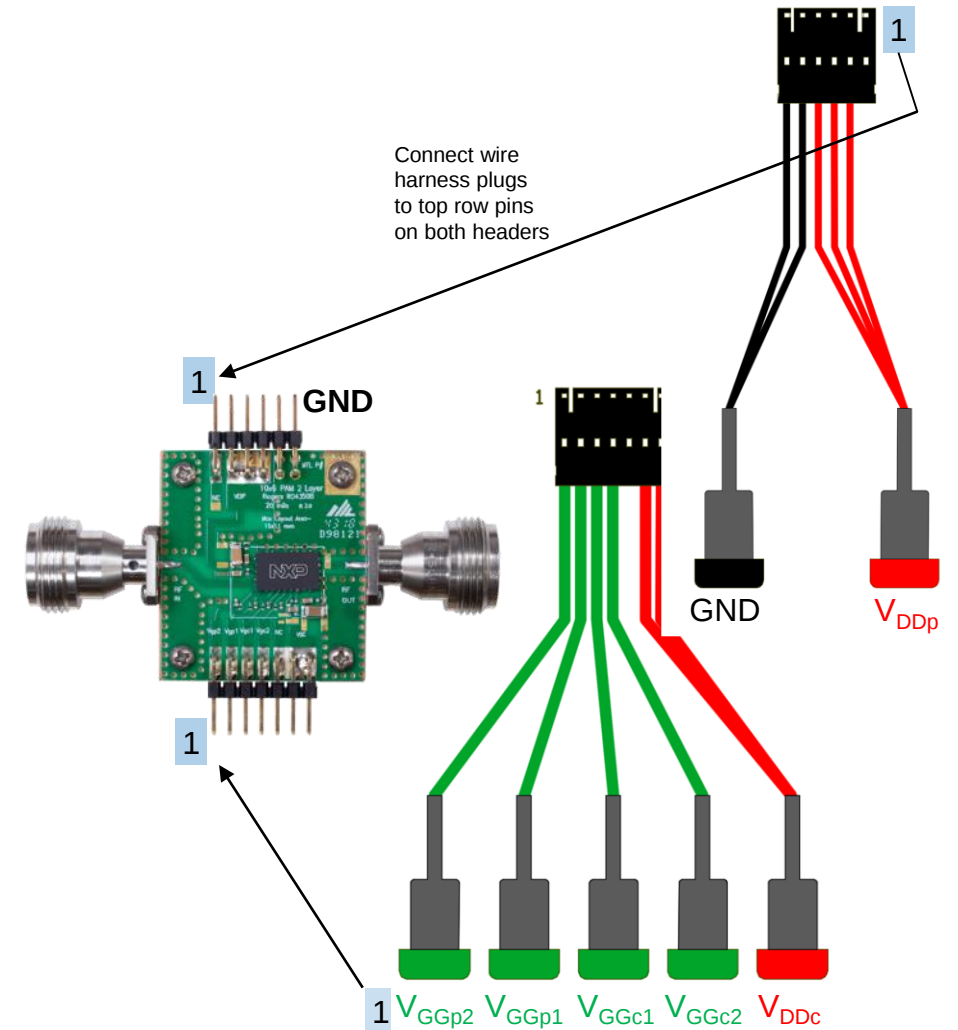
- Labeling:

V_{GSc1} : gate voltage for carrier driver
 V_{GSc2} : gate voltage for carrier final stage
 V_{GSp1} : gate voltage for peaking driver
 V_{GSp2} : gate voltage for peaking final stage
 V_{DSc1} : drain voltage for carrier driver
 V_{DSc2} : drain voltage for carrier final stage
 V_{DSp1} : drain voltage for peaking driver
 V_{DSp2} : drain voltage for peaking final stage
 I_{DQc1} : quiescent current for carrier driver
 I_{DQc2} : quiescent current for carrier final stage
 V_{DSc2} and V_{DSp2} are DC coupled internal to the package

Reference Circuit Connection Details

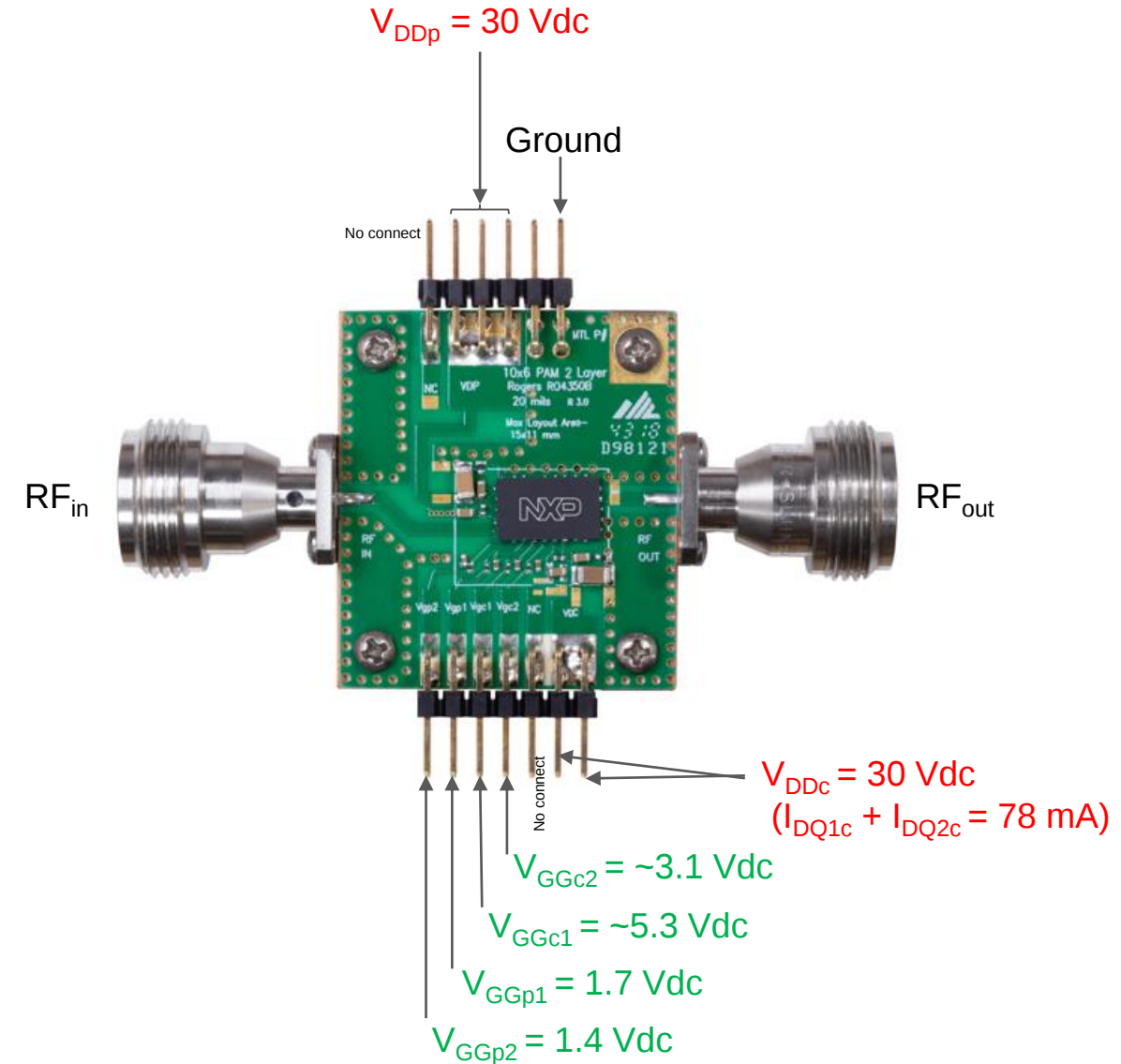


- Labeling:
 - V_{GGc1} : fixture gate voltage for carrier driver
 - V_{GGc2} : fixture gate voltage for carrier final stage
 - V_{GGp1} : fixture gate voltage for peaking driver
 - V_{GGp2} : fixture gate bias voltage for peaking final stage
 - V_{DDc} : fixture drain voltage for both V_{DSc1} and V_{DSc2}
 - V_{DDp} : fixture drain voltage for both V_{DSp1} and V_{DSp2}

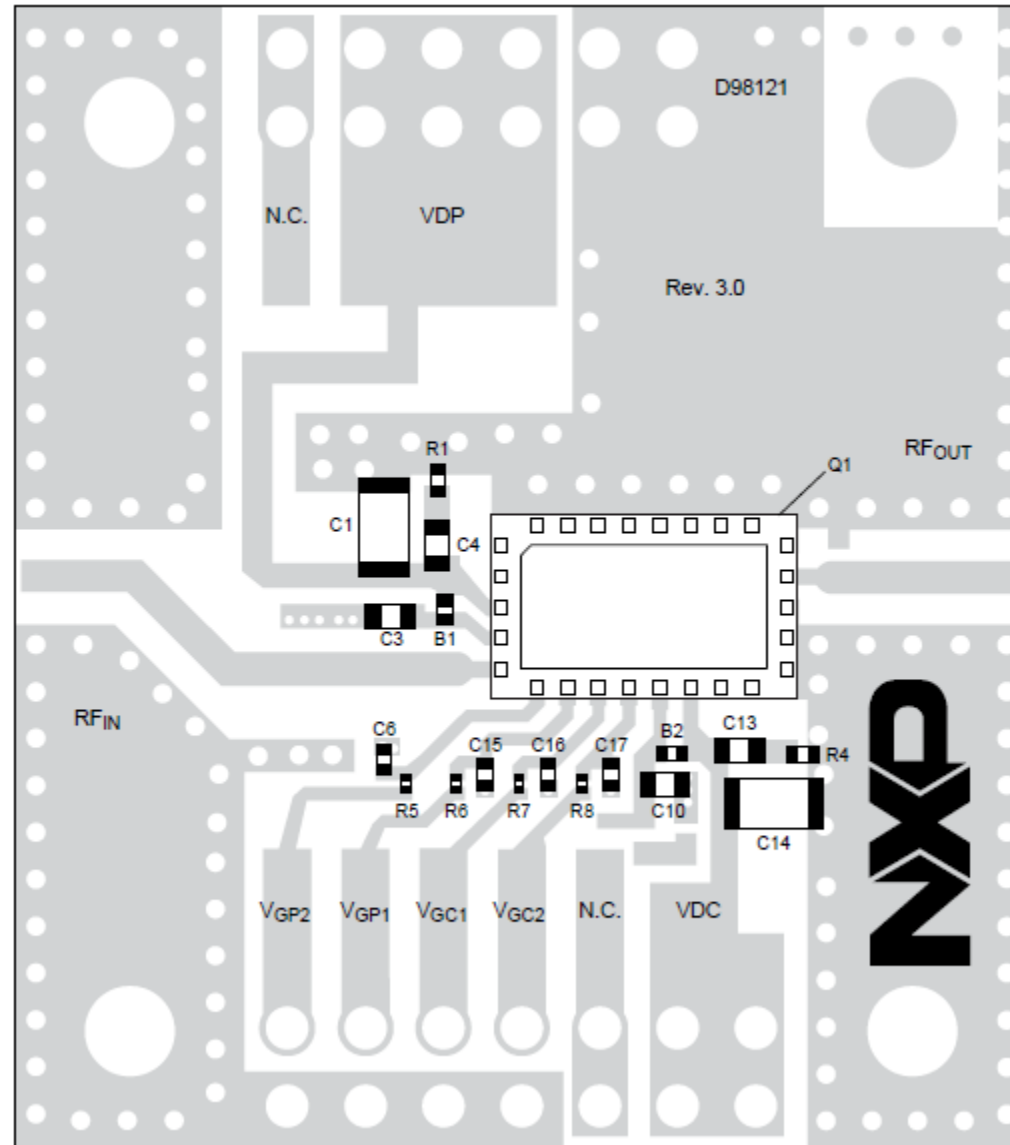


Quick Start

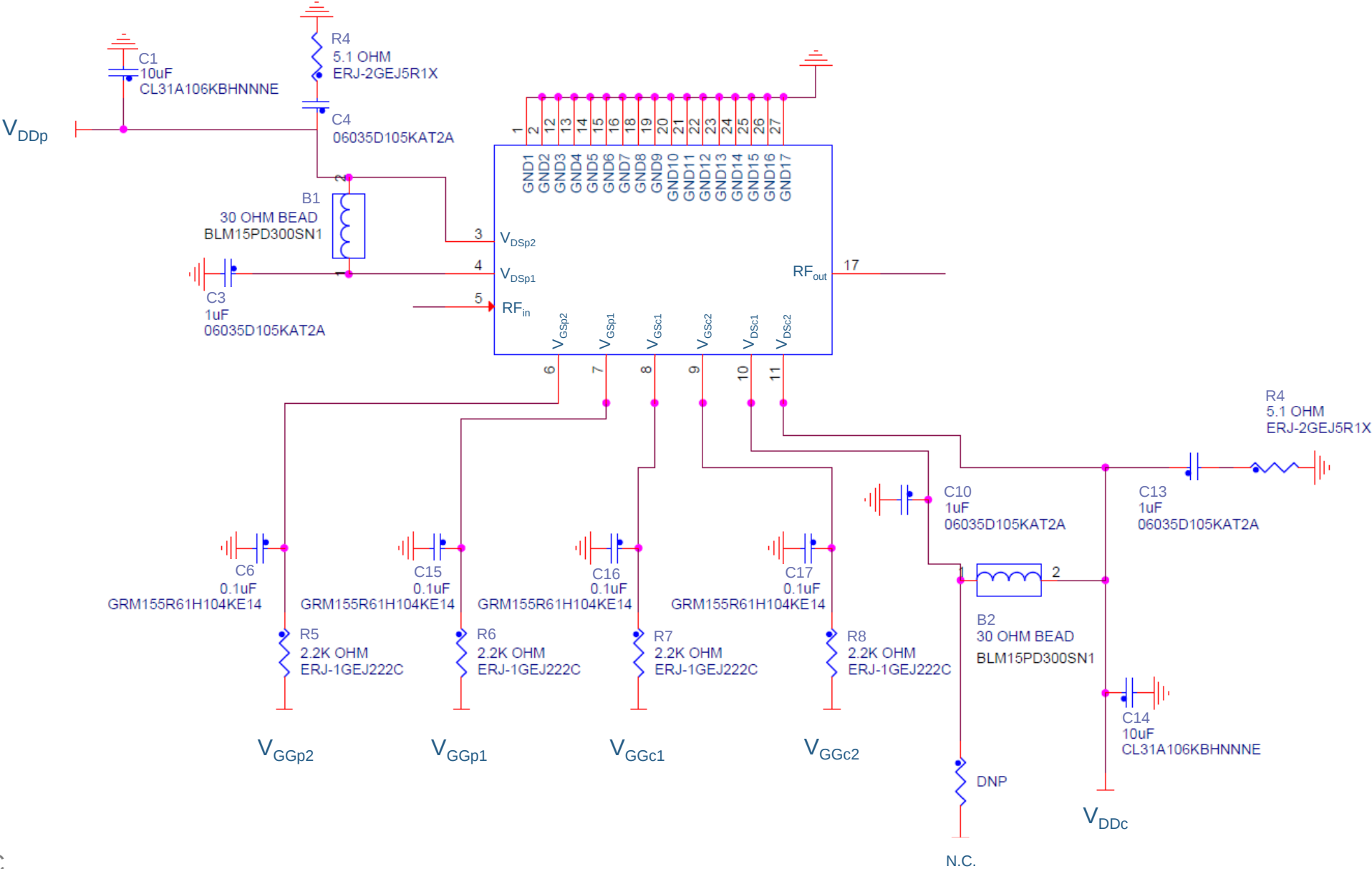
1. Mount the reference circuit onto a heatsink capable of dissipating more than 8 W in order to provide enough thermal dissipation (the baseplate included in this reference circuit is not sufficient to serve as a standalone heatsink).
2. Connect the ground.
3. Terminate the RF output with a 50 ohm load capable of handling more than 36 W peak power.
4. Connect the RF input to a 50 ohm source with the RF off.
5. Connect the carrier drain voltage (V_{DDc}) and the peaking drain voltage (V_{DDp}) and raise them slowly to 30 V in no particular order. Current should be 0 A.
6. Connect the gate voltage for the carrier driver (V_{GGc1}) and raise it slowly to the typical carrier driver's quiescent current of $I_{DQc1} = 17.5$ mA. V_{GGc1} should be around 5.3 V.
7. Set V_{GGc1} to 0 V. Connect the gate voltage for the carrier final stage (V_{GGc2}) and raise it slowly to the carrier final stage's quiescent current of $I_{DQc2} = 60.5$ mA. V_{GGc2} should typically be around 3.1 V.
8. Set V_{GGc1} and V_{GGc2} to the values found in steps 6 and 7. The total quiescent current $I_{DQc1} + I_{DQc2}$ should be around 78 mA.
9. Set V_{GGp1} at 1.7 V and V_{GGp2} at 1.4 V.
10. Raise the RF input slowly to 6 mW (7.7 dBm).
11. Check the RF output power (typically 5 W avg), the drain current (around 425 mA for this power level) and the temperature of the board.



Component Placement Reference



Schematics



Bill of Materials

Part	Description	Part Number	Manufacturer
B1, B2	30 Ω Ferrite Bead	BLM15PD300SN1	Murata
C1, C14	10 μ F Chip Capacitor	CL31A106KBHNNNE	Samsung
C3, C4, C10, C13	1 μ F Chip Capacitor	06035D105KAT2A	AVX
C6, C15, C16, C17	0.1 μ F Chip Capacitor	GRM155R61H104KE14	Murata
Q1	Power Amplifier Module	AFSC5G35D37	NXP
R1, R4	5.1 Ω , 1/10 W Chip Resistor	ERJ-2GEJ5R1X	Panasonic
R5, R6, R7, R8	2.2 k Ω , 1/20 W Chip Resistor	ERJ-1GEJ222C	Panasonic
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.67$	D98121	MTL

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.

Revision History

- The following table summarizes revisions to the content of the AFSC5G35D37 3400-3600 MHz Reference Circuit zip file.

Revision	Date	Description
0	September 2019	• Initial Release



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